AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising:

configurable system logic having programmable logic;

a direct memory access (DMA) controller adapted to operate in a descriptor mode;

a configurable system interconnect coupled between the configurable system logic and the DMA controller; [[and]]

an input/output (I/O) device coupled to the DMA controller by way of the configurable system interconnect, wherein the I/O device is implemented in the programmable logic and the DMA controller terminates a DMA transfer and clears a current transfer counter before a terminal count is reached upon receiving an early termination request signal from the I/O device, and wherein the DMA controller sends an acknowledge signal to the I/O device in response to receiving the early termination request signal; and

a descriptor table storing commands to carry out a transfer, the descriptor table being updated with a reduced transfer count in response to receiving the early termination request signal from the I/O device when the DMA controller is operating in the descriptor mode.

2. (Previously Presented) The system of claim 1 wherein the DMA controller re-executes a DMA transfer with the I/O device upon receiving a retransmit request signal from the I/O device.

Claims 3-5. (Cancelled)

6. (Previously Presented) The system of claim 1 further comprising:

a central processing unit (CPU) coupled to the system interconnect; and

a memory device coupled to the system interconnect.

Claims 7-11. (Cancelled)

12. (Currently Amended) A system comprising:

configurable system logic having programmable logic;

a direct memory access (DMA) controller adapted to operate in a descriptor mode;

a configurable system interconnect coupled between the configurable system logic and the DMA controller; [[and]]

a descriptor table storing commands to carry out a transfer of data with the DMA controller; and

an input/output (I/O) device coupled to the DMA controller, wherein the I/O device is implemented in the programmable logic and the DMA controller re-executes a DMA transfer of the data associated with a current descriptor entry stored in the descriptor table from the beginning with the I/O device upon receiving a retransmit request signal from the I/O device, and wherein the DMA controller sends an acknowledge signal to the I/O device in response to receiving the retransmit request signal and the transmission of the data associated with the current descriptor entry stored in the descriptor table is restarted.

13. (Currently Amended) A method comprising:

configuring a first device in programmable logic of an integrated circuit;

coupling the first device to a configurable system interconnect;

transferring data between the first device and a second device under control of a direct memory access (DMA) controller by way of the configurable system interconnect;

storing commands in a descriptor table to carry out a transfer of data between the first device and the second device;

receiving a request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device in response to receiving the request by the first device to re-transmit the data; and

re-transferring the data associated with a current descriptor entry stored in the descriptor table from the beginning between the first device and the second device.

14. (Original) The method of claim 13 further comprising reloading configuration registers within the DMA controller prior to transmitting the acknowledge signal to the first device.

15. (Currently Amended) A method comprising:

configuring a first device in programmable logic of an integrated circuit;

coupling the first device to a configurable system interconnect;

storing commands in a descriptor table to carry out a transfer of data between the first device and a second device;

transferring data between the first device and [[a]] the second device under control of a direct memory access (DMA) controller by way of the configurable system interconnect;

receiving a request signal at the DMA controller from the first device indicating a request by the first device to terminate the transfer of data between the first device and the second device;

erasing appropriate DMA controller information in order to restart the transfer of data between the first device and the second device;

transmitting an acknowledge signal from the DMA controller to the first device in response to receiving the request by the first device to terminate the transfer of data; [[and]]

terminating the transfer of data between the first device and the second device; and

updating the descriptor table with a reduced transfer count in response to receiving the request by the first device to terminate the transfer of data when the direct memory access controller is operating in the descriptor mode.

16. (Previously Presented) The method of claim 15 wherein the erasing comprises, clearing a counter within the DMA controller prior to transmitting the acknowledge

signal to the first device.

Claims 17-20. (Cancelled)

21. (Previously Presented) The method of claim 15 further comprising:

receiving a second request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

re-transferring the data between the first device and the second device according to the first set of commands.

22. (Previously Presented) The method of claim 15 further comprising:

receiving a second request signal at the DMA controller from the first device indicating a request by the first device to re-transmit the data between the first device and the second device;

transmitting a second acknowledge signal from the DMA controller to the first device; and

terminating the transfer of data between the first device and the second device.

Claim 23. (Cancelled)

24. (Previously Presented) The system of claim 1 wherein the DMA controller comprises a first channel coupled to the I/O device to facilitate the transfer of data.

25. (Previously Presented) The system of claim 24 wherein the DMA controller further comprises a register, coupled to the channel, to store configuration data.

26. (Previously Presented) The system of claim 25 wherein the DMA controller further comprises error checking logic.

27. (Previously Amended) The system of claim 24 wherein the channel comprises control logic to control the transfer process within the first channel.

Claim 28. (Cancelled)

29. (Previously Presented) The system of claim 12 wherein the DMA controller comprises a first channel coupled to the I/O device to facilitate data transfers.

30. (Previously Presented) The system of claim 29 wherein the DMA controller further comprises a register, coupled to the channel, to store configuration data.

31. (Previously Presented) The system of claim 30 wherein the DMA controller further comprises error checking logic.

32. (Previously Presented) The system of claim 29 wherein the channel comprises control logic to control the transfer of data.